REMARKS

The present response amends the specification to correct a typographical error. Claims 1-22 are pending in the captioned case. Applicants respectfully request further examination and reconsideration of the presently claimed application.

Section 102 Rejection

Claims 1, 2, 9-14, and 16-20 were rejection under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 6,201,829 to Schneider (hereinafter "Schneider"). The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art of reference. *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); MPEP 2131. Furthermore, anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, as arranged in the claim. *W.L. Gore & Assocs. V. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983). Using these standards, Applicants submit the cited art fails to disclose each and every element of the currently pending claims, some distinctive features of which are set forth in more detail below.

Schneider does not teach or suggest a random bit generator adapted to produce a random pattern of bits in parallel onto *n* conductors (claim 1), a serializer coupled to receive a random pattern of *m* bits clocked in parallel upon *n* conductors (claim 9), or simply generating a random pattern of bits and serializing the random pattern of bits (claim 19). Each of the present independent claims 1, 9, and 19 set forth a random pattern generator, a serializer coupled to receive a random pattern of bits produced from such generator, or simply serializing a random pattern of bits. As described in the present specification, conventional built-in self-test (BIST) testers either utilize all 0s and/or all 1s bit pattern, walking 0s or walking 1s bit patterns, or a combination of each. Using the sequentially shifted set of walking 0s and/or 1s is, however, not a pure random bitstream (Specification -- pg. 4, lines 9-14). Instead, walking 0s and walking 1s shifted from the least significant bit position to the most significant bit position within a parallel set of conductors represents what most people skilled in art refer to as "pseudo-random bit generators."

A pseudo-random bit generator or PRBG is dependent on serial shifting of 1s or 0s and, thus, a particular pattern is required for testing a target device. As described in the present specification, "this type of test is not only non-robust, but also cannot test a fuller pattern of bits that would normally be presented to the serializer and deserializer during its operation." (Specification – pg. 4, lines 12-14.) Instead, it would be desirable to implement the present claims of a pure random bit generator that is not dependent on a particular pattern of shifting 1s or 0s applicable to PRBGs.

Contrary to a pure random bit generator, the primary reference to Schcider clearly discloses and is limited to a pseudo-random bit generator, dependent on marching 0s from the least significant bit position to the most significant bit position (Schneider – Fig. 3). Unfortunately, however, as described in Schneider, pure pseudo-random bit generators must be modified in order to accommodate what Schneider refers to as the Fibre-Channel 8B/10B transmission code being placed on the parallel conductors (Schneider -- col. 2, lines 1-14). The 8B/10B transmission coding scheme cannot accommodate more than five sequential 1s or 0s and, thus, the marching 0s pseudo-random bit generator must be modified further (Schneider – Figs. 6 and 7; col. 2, lines 41-52; col. 4, lines 54-59; col. 5, lines 1-6). While implementing a marching 0s pattern, Schneider further teaches that within its pseudo-random bit generator, the least significant bit and fifth least significant bit positions must be inverted to prevent a pattern having more than five sequential 1s or 0s. Again, however, the generated bit pattern is not random as presently claimed. Instead, to accommodate the Fiber-Channel 8B/10B transmission code, the generator is limited to a pattern of marching 0s with the 0 and fifth bit patterns inverted. This simply is not a random bit generator, and cannot be modified to achieve a random bit generator as presently claimed. If any modifications are attempted, then the purpose of Schneider accommodating an 8B/10B encoding scheme would be entirely defeated.

In addition to the patentable distinctions of the independent claims, as will be set forth below, several dependent claims are also patentably distinguishable over Schneider.

Schneider does not teach or suggest a relay coupled to connect the loop back conductor between the serializer and the deserializer. Present claim 11 specifically recites the inclusion of a relay and, more specifically, a relay coupled to connect a loop back conductor. Contrary to the assertions made in the Office Action, Schneider makes no mention whatsoever of a relay and, certainly, not a relay coupled to connect a loop back conductor between a serializer and a deserializer (Schneider -- col. 7, lines 58-63). Instead, Schneider clearly describes a multiplexer – not a relay. Applicants content that one skilled in the art would appreciate the difference between a relay and a multiplexer.

Schneider does not teach a portion of a serializer, deserializer, and comparator comprising a programmable logic device (PLD). Present claim 17 recites the serializer, deserializer, and comparator at least partially formed within a programmable logic device. Instead of having the serializer, deserializer, and comparator forming a PLD, Schneider specifically requires the mode signal be derived external from the serializer, deserializer, and comparator; more importantly, the mode signal is sent from a controller circuitry operating in software or firmware (Schneider – Fig. 5; col. 7, lines 30-35). In fact, Schneider makes clear that the programmable mode signal can be sent from a PLD to a serializer and deserializer, thus, making the PLD be outside and exclusive from the serializer and deserializer.

For the foregoing reasons, Applicants assert that each of the present independent claims and claims dependent therefrom are patentably distinct over the teachings of Schneider. Accordingly, Applicants respectfully request removal of this rejection.

Section 103 Rejection

Claims 3-8, 15, 21, and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over various references. In particular, the Office Action alleges that these dependent claims are unpatentable over Schnieder in view of U.S. Patent No. 5,444,645 to Yoshida et al. (hereinafter "Yoshida"), U.S. Patent No. 4,941,082 to Pailthorp et al. (hereinafter "Pailthorp"), U.S. Patent No. 6,094,532 to Acton et al. (hereinafter "Acton"), U.S. Patent Application Publication No. 2002/0147611 to Greene et al. (hereinafter "Greene"), and an article entitled "SCAN921023 and SCAN921224 20-66 MHz 10 Bit Bus LVDS Serializer and Deserializer with IEEE 1149.1 (JTAG) and at-speed BIST" by National Semiconductor Corp. ("NSC Article"). Applicants respectfully traverse this rejection.

To establish a case of *prima facie* obviousness of a claimed invention, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Second, there must be a reasonable expectation of success. As stated in MPEP 2143.01, the fact that references can be hypothetically combined or modified is not sufficient to establish a *prima facie* case of obviousness. *See In re Mills*, 916 F.2d. 680 (Fed. Cir. 1990). Finally, the prior art references must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d. 981 (CCPA 1974); MPEP 2143.03. Specifically, "all words in a claim must be considered when judging the patentability of that claim against the prior art." *In re Wilson* 424 F.2d., 1382 (CCPA

1970). Using these standards, Applicants contend that the cited art fails to teach or suggest all features of the currently pending claims, some distinctive features of which are set forth in more detail below.

In addition to the patentable distinctions of the independent claims described in response to the § 102 rejections, several dependent claims are also patentably distinguishable over the cited art.

Schneider and the NSC Article do not teach or suggest, either singularly or in combination, a test access port adapted to receive an instruction to the random bit generator for signaling production of the random pattern of bits. Present dependent claims 6, 7, 21, and 22 make clear that a test access port compliant with IEEE Std. 1149.1 is recited in the present claims. Moreover, the test access port is claimed to receive an instruction used to signal production of a random pattern of bits from the random pattern generator. Contrary to a test access port used to receive an instruction, the test access port of the NCS Article clearly describes receiving test data input – i.e., data, not instructions (NSC Article -- pg. 1, first paragraph). Nowhere is there any suggestion in the NSC Article that the TDI input to the test access port can accommodate instruction. Moreover, their certainly is no teaching that one of such instructions be that which instructs a random bit generator to produce a random pattern of bits.

For at least the reasons set forth above with respect to the § 103 rejection, and those presented in response to the § 102 rejection, Applicants assert that the present independent claims and claims dependent therefrom are patentable over the cited art. Accordingly, Applicants request removal of this rejection.

CONCLUSION

The present amendment and response is believed to be a complete response to the issues raised in the Office Action mailed May 6, 2004. In view of the remarks traversing the rejections, Applicants assert that claims 1-22 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to Conley Rose, P.C. Deposit Account No. 03-2769/5298-06300.

Respectfully submitted,

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